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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,697	01/02/2004	Dinkar Singh	Y0R920010768US2	3821
24299	7590	03/30/2005		EXAMINER
George Sai-Halasz 145 Fernwood Dr. Greenwich, RI 02818				PRENTY, MARK V
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/750,697	SINGH ET AL.
	Examiner MARK V. PRENTY	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 02 January 2004.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-13 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1,2 and 7-10 is/are rejected.

7)  Claim(s) 3-13 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 02 January 2004 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date *July 14, 2004*.  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. *\_\_\_\_\_*.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: *\_\_\_\_\_*.

This Office Action is in response to the papers filed on January 2, 2004.

Independent claim 7 is objected to because "said enchanted T-gate" (line 1) should read, "said enhanced T-gate." Correction is required. Claim 8 depends on independent claim 7 and is thus similarly objected to.

Independent claim 9 is objected to because "said enchanted T-gate" (line 2) should read, "said enhanced T-gate." Correction is required. Claims 10-13 depend on independent claim 9 and are thus similarly objected to.

Claims 1 and 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent 6,822,307 to Nihei et al. (Nihei).

With respect to independent claim 1, Nihei discloses an enhanced T-gate (see the entire patent, including the Fig. 1 disclosure, for example) comprising: a free T-gate 15, said free T-gate having a neck portion 15A-15C, said neck portion having a height, and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion by a first width; and an insulator layer 18 disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Nihei.

With respect to independent claim 7, Nihei discloses a MODFET device comprising an enhanced T-gate, said [enhanced] T-gate further comprising: a free T-

gate 15, said free T-gate having a neck portion 15A-15C and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and an insulator layer 18 disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Nihei.

With respect to dependent claim 8, Nihei's device further comprises a self-aligned source/drain metallurgy 16/17, wherein a borderline of said metallurgy is defined by said insulator layer 18.

Claim 8 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Nihei.

With respect to independent claim 9, Nihei discloses an integrated circuit comprising at least one MODFET device, said MODFET device comprising an enhanced T-gate, wherein said [enhanced] T-gate further comprising: a free T-gate 15, said free T-gate having a neck portion 15A-15C and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and an insulator layer 18 disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 9 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Nihei.

With respect to dependent claim 10, Nihei's MODFET further comprises a self-aligned source/drain metallurgy 16/17, wherein a borderline of said metallurgy is defined by said insulator layer 18.

Claim 10 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Nihei.

Claims 1 and 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent 6,605,831 to Inai et al. (Inai).

With respect to independent claim 1, Inai discloses an enhanced T-gate (see the entire patent, including the Fig. 1 disclosure, for example) comprising: a free T-gate 10, said free T-gate having a neck portion, said neck portion having a height, and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion by a first width; and an insulator layer 11 disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Inai.

With respect to independent claim 7, Inai discloses a MODFET device comprising an enhanced T-gate, said [enhanced] T-gate further comprising: a free T-gate 10, said free T-gate having a neck portion and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and an insulator layer 11 disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only

partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Inai.

With respect to dependent claim 8, Inai's device further comprises a self-aligned source/drain metallurgy 8/9, wherein a borderline of said metallurgy is defined by said insulator layer 11.

Claim 8 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Inai.

With respect to independent claim 9, Inai discloses an integrated circuit comprising at least one MODFET device, said MODFET device comprising an enhanced T-gate, wherein said [enhanced] T-gate further comprising: a free T-gate 10, said free T-gate having a neck portion and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and an insulator layer 11 disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 9 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Inai.

With respect to dependent claim 10, Inai's MODFET further comprises a self-aligned source/drain metallurgy 8/9, wherein a borderline of said metallurgy is defined by said insulator layer 11.

Claim 10 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Inai.

Claims 1, 2, 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent 5,734,185 to Iguchi et al. (Iguchi).

With respect to independent claim 1, Iguchi discloses an enhanced T-gate (see the entire patent, including the Fig. 9 disclosure, for example) comprising: a free T-gate 19, said free T-gate having a neck portion, said neck portion having a height, and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion by a first width; and an insulator layer 16b disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Iguchi.

With respect to dependent claim 2, wherein in Iguchi's sandwich structure said insulator layer 16b creating spacers on each side of said neck portion, wherein said spacers having a second width, said second width being less than said first width of said overhangs, whereby that part of said volume which is further from said neck portion than said second width is not filled with said insulators.

Claim 2 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Iguchi.

With respect to independent claim 7, Iguchi discloses a MOSFET<sup>1</sup> device comprising an enhanced T-gate, said [enhanced] T-gate further comprising: a free T-

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<sup>1</sup> Independent claim 7's "MODFET" preamble language is not given patentable weight. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

gate 19, said free T-gate having a neck portion and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and an insulator layer 16b disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 7 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Iguchi.

With respect to independent claim 9, Iguchi discloses an integrated circuit comprising at least one MOSFET<sup>2</sup> device, said MOSFET device comprising an enhanced T-gate, wherein said [enhanced] T-gate further comprising: a free T-gate 19, said free T-gate having a neck portion and a T-bar portion, said T-bar portion having overhangs extending beyond said neck portion; and an insulator layer 16b disposed on each side of said neck portion, forming a sandwich structure with said neck portion along a width direction of said free T-gate, and wherein said insulator layer only partially filling up a volume defined therebetween said overhangs and a surface on which said free T-gate is standing.

Claim 9 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Iguchi.

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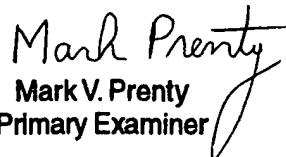
<sup>2</sup> Independent claim 9's "MODFET" preamble language is not given patentable weight. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claims 3-6 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

United States Patent 6,740,535 to Singh et al. is related to this application.

The prior art of record does not disclose or suggest the allowable structures taken as a whole, including the insulator layer.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

  
Mark V. Prenty  
Primary Examiner